Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims (marked version):

1. (Currently Amended) A circuit of a continuous-time filter comprises:

a forward transmission delay line configured to have at least one forward transmission line delay element with corresponding at least one forward delay-time;

an input signal coupled to an input of the transmission delay line; a first termination impedance coupled to an output of the forward transmission delay line and configured to terminate the forward transmission delay line;

a first forward transconductance element coupled to the input signal and configured to multiply the input signal by a first forward filter coefficient and to convert the input signal to a first forward current;

at least one second forward transconductance element coupled to at least one corresponding forward output of the at least one forward transmission line delay element and configured to multiply at least one time-delayed input signal by at least one corresponding forward filter coefficient and to convert at least one multiplied forward time-delayed input signal to at least one second forward current;

~~an~~ forward output of the first forward transconductance element and at least one second corresponding forward output of the at least one second forward transconductance element coupled together to form a current summing node for summing the first forward current and the at least one second forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed continuous current to a filtered output voltage signal.

a feedback transmission delay line configured to have at least one feedback transmission line delay element configured to have corresponding at least one feedback delay-time;

the filtered output voltage signal coupled back to a feedback input of the feedback transmission delay line;

a second termination impedance coupled to an output of the feedback transmission delay line and configured to terminate the feedback transmission delay line;

at least one feedback transconductance element coupled to corresponding at least one output of the at least one feedback transmission line delay element and configured to multiply at least one time-delayed output signal by corresponding at least one feedback filter coefficient and convert at least one multiplied time-delayed output signal to at least one feedback current; and

at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

2. (Previously Amended) The circuit of claim 1 wherein the input signal is single ended or differential and the output voltage signal is single ended or differential.

3. (Previously Amended) The circuit of claim 1 wherein the said transmission line delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a semiconductor substrate, on a package substrate or on a printed circuit board (PCB).

4. (Previously Amended) The circuit of claim 1 wherein each of the said transmission line delay elements has a fixed or a programmable delay time.

5. (Previously Amended) The circuit of claim 1 wherein the transmission delay line comprises a fixed or programmable number of transmission line delay elements.

6. (Previously Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured as a transconductance amplifier, as a multistage voltage amplifier, resistors, or a combination of resistors and voltage amplifiers.

7. (Previously Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured to have a fixed value, a programmable value, or an adaptively controlled value.

8. (Cancelled)

9. (Previously Amended) The circuit of claim 1 wherein the termination impedance is configured to have a matched or mismatched impedance in response to a system filter requirement specification.

10. (Previously Amended) The circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for a fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Previously Amended) The circuit of claim 1 further comprises input matching impedance elements configured for matching to the corresponding inputs of the said transconductance elements.

12.-14. (Cancelled)

15. (Currently Amended) The circuit of claim 1 wherein the analog filter is configured as an infinite impulse response (IIR) filter for equalizing an input signal in disk drives, optical , serial chip-to-chip, serial backplane high speed networks, or radio frequency communication systems.

16-30. (Cancelled)

Listing of Claims (clean version):

1. (Currently Amended) A circuit of a continuous-time filter comprises:

a forward transmission delay line configured to have at least one forward transmission line delay element with corresponding at least one forward delay-time;

an input signal coupled to an input of the transmission delay line; a first termination impedance coupled to an output of the forward transmission delay line and configured to terminate the forward transmission delay line;

a first forward transconductance element coupled to the input signal and configured to multiply the input signal by a first forward filter coefficient and to convert the input signal to a first forward current;

at least one second forward transconductance element coupled to at least one corresponding forward output of the at least one forward transmission line delay element and configured to multiply at least one time-delayed input signal by at least one corresponding forward filter coefficient and to convert at least one multiplied forward time-delayed input signal to at least one second forward current;

a forward output of the first forward transconductance element and at least one second corresponding forward output of the at least one second forward transconductance element coupled together to form a current summing node for summing the first forward current and the at least one second forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed continuous current to a filtered output voltage signal.

a feedback transmission delay line configured to have at least one feedback transmission line delay element configured to have corresponding at least one feedback delay-time;

the filtered output voltage signal coupled back to a feedback input of the feedback transmission delay line;

a second termination impedance coupled to an output of the feedback transmission delay line and configured to terminate the feedback transmission delay line;

at least one feedback transconductance element coupled to corresponding at least one output of the at least one feedback transmission line delay element and configured to multiply at least one

time-delayed output signal by corresponding at least one feedback filter coefficient and convert at least one multiplied time-delayed output signal to at least one feedback current; and
at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

2. (Previously Amended) The circuit of claim 1 wherein the input signal is single ended or differential and the output voltage signal is single ended or differential.

3. (Previously Amended) The circuit of claim 1 wherein the said transmission line delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a semiconductor substrate, on a package substrate or on a printed circuit board (PCB).

4. (Previously Amended) The circuit of claim 1 wherein each of the said transmission line delay elements has a fixed or a programmable delay time.

5. (Previously Amended) The circuit of claim 1 wherein the transmission delay line comprises a fixed or programmable number of transmission line delay elements.

6. (Previously Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured as a transconductance amplifier, as a multistage voltage amplifier, resistors, or a combination of resistors and voltage amplifiers.

7. (Previously Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured to have a fixed value, a programmable value, or an adaptively controlled value.

8. (Cancelled)

9. (Previously Amended) The circuit of claim 1 wherein the termination impedance is configured to have a matched or mismatched impedance in response to a system filter requirement specification.

10. (Previously Amended) The circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for a fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Previously Amended) The circuit of claim 1 further comprises input matching impedance elements configured for matching to the corresponding inputs of the said transconductance elements.

12.-14. (Cancelled)

15. (Currently Amended) The circuit of claim 1 wherein the analog filter is configured as an infinite impulse response (IIR) filter for equalizing an input signal in disk drives, optical , serial chip-to-chip, serial backplane high speed networks, or radio frequency communication systems.

16-30. (Cancelled)